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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,579	02/27/2002	Ravi Nair	YOR920010219US2	5881
21254	7590	08/24/2004	EXAMINER	
MCGINN & GIBB, PLLC			CHU, GABRIEL L	
8321 OLD COURTHOUSE ROAD				
SUITE 200			ART UNIT	PAPER NUMBER
VIENNA, VA 22182-3817			2114	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/083,579	NAIR ET AL.
	Examiner Gabriel L. Chu	Art Unit 2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 25 April 2002.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 7-21 is/are allowed.

6) Claim(s) 1-6 and 23-25 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6499048 to Williams. Referring to claim 1, Williams discloses a method of multithread processing on a computer, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, "The invention finds application, for example, to a single processor configured to process multiple threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit

may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism.”).

Referring to claim 2, Williams discloses generating a fault signal if said comparison is not equal (From line 64 of column 3, “If just two processing sets are used, or if following elimination of one or more faulty processing sets only two valid processing sets remain operable, a difference between the operation of the processing sets can signal faulty operation of one of the processing sets, although identification of which one of the processing sets is faulty can be a more complex task than simply employing majority voting.”).

Referring to claim 3, Williams discloses providing an input to enable or to disable said method (From line 64 of column 3, “If just two processing sets are used, or if following elimination of one or more faulty processing sets only two valid processing sets remain operable, a difference between the operation of the processing sets can signal faulty operation of one of the processing sets, although identification of which one of the processing sets is faulty can be a more complex task than simply employing majority voting.”).

Referring to claim 4, Williams discloses said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component (From line 35 of column 5, “The progress indication is used by the monitor to slow down a processor so that it

does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.”).

Referring to claim 5, Williams discloses said processing said thread on said second component occurs at a time delayed from that of said processing said thread on said first component (From line 35 of column 5, “The progress indication is used by the monitor to slow down a processor so that it does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.”).

Referring to claim 6, Williams discloses said processing said thread on said second component uses information available from said processing said thread on said first component (From line 35 of column 5, “The progress indication is used by the monitor to slow down a processor so that it does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.”).

Referring to claim 23, Williams discloses A multiprocessor system executing a method of multithread processing on a computer, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, “The invention finds application, for example, to a single processor configured to process multiple threads, or

processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors.

Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism.”).

Claim Rejections - 35 USC § 103

3. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6499048 to Williams. Referring to claim 24, Williams discloses a medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus (From the abstract, “A program controlled apparatus...”) to perform a method of multithread processing, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, “The invention finds application, for example, to a single processor configured to process multiple threads, or

processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors.

Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism."). Although Williams does not specifically disclose this medium can be an Application Specific Integrated Circuit (ASIC), using an ASIC to implement a method is notoriously well known in the art. Examiner takes official notice for ASICs. A person of ordinary skill in the art at the time of the invention would have been motivated to implement a method because ASICs improve performance over general-purpose CPUs, because ASICs are "hardwired" to do a specific job and do not incur the overhead of fetching and interpreting stored instructions.

Referring to claim 25, Williams discloses a medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus (From the abstract, "A program controlled apparatus...") to perform a method of multithread processing, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least

two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, “The invention finds application, for example, to a single processor configured to process multiple threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism.”). Although Williams does not specifically disclose this medium can be a Read Only Memory (ROM), using a ROM to implement a method is notoriously well known in the art. A person of ordinary skill in the art at the time of the invention would have been motivated to use a ROM because the person does not want the instructions to change and because ROM is non-volatile.

Allowable Subject Matter

4. Claims 7-21 are allowed.

5. The following is an examiner’s statement of reasons for allowance:

Referring to claims 7-12, the prior art does not teach or fairly suggest wherein said first background thread executes a check on said second foreground thread

and said second background thread executes a check on said first foreground thread, thereby achieving a crosschecking of said first SMT processor and said second SMT processor, in the scope and context of claim 7.

Referring to claims 13-21, the prior art does not teach or fairly suggest wherein said first background thread executes a check on said second foreground thread and said second background thread executes a check on said first foreground thread, in the scope and context of claim 13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5138708 to Vosbury

US 5388242 to Jewett

US 5452443 to Oyamada et al.

US 5764660 to Mohat

US 5896523 to Bissett et al.

US 6385755 to Shimomura et al.

US 6757811 to Mukherjee

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is

(703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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